2183

Patent

Docket No.: CYPR-CD00232

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.					
Date of Deposit:	4/7/05	Name of Person Making the Deposit:	Luz Castillo	Signature of the Person Making the Deposit:	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Snyder — Group Art Unit: 2183

Filed: October 22, 2001 — Examiner: PAN, Daniel H.

Application No.: 10/033,027

Confirmation No.: 8635

Title: PROGRAMMABLE SYSTEM ON A CHIP

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

_____ Formal drawings, totaling _____ sheets.
_____ Informal drawings, totaling _____ sheets.
X Certification for PTO Consideration
X Information Disclosure statement (2 sheets)
_____ Information Disclosure statement and late filing fee
X Form 1449
_____ Petition for Extension of Time
_____ Other: _____

Fee Calculation (for other than a small entity)					
Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	
Information Disclosure Statement, late filing				$180.00	
Other:					
Total Fees					0.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[ ] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $

[X] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

kgr 7/98

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 000041066

Respectfully submitted,

Date: April 6, 2005

By: _____
Anthony C. Murabito
Reg. No. 35, 295

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: CYPR-CD00232

Inventor(s): Snyder

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Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
5,399,922	MACROCELL COMPRISED OF TWO LOOK-UP TABLES AND TWO FLIP-FLOPS	Mar. 21, 1995
5,680,070	PROGRAMMABLE ANALOG ARRAY AN METHOD FOR CONFIGURING THE SAME	Oct. 21, 1997

FOREIGN DOCUMENTS

Document No.:	Title:	Publ. Date
EP 0 450 863 A2	INTEGRATED CIRCUIT FOR ANALOG SYSTEM	Oct. 9, 1991
EP 0 499 383 A2	MIXED MODE ANALOG/DIGITAL PROGRAMMABLE INTERCONNECT ARCHITECTURE	Aug. 19, 1992
EP 0 308 583 A2	DIGITAL COMPUTER HAVING SIGNAL CIRCUITRY	Mar. 29, 1989
EP 0 639 816 A2	FIELD PROGRAMMABLE DIGITAL SIGNAL PROCESSING ARRAY INTEGRATED CIRCUIT	Feb. 22, 1995

EP 1 170 671 A1	PROGRAMMABLE ANALOG ARRAY CIRCUIT	Jan. 9, 2002
PCT WO 95/32478	INTEGRATED CIRCUIT HAVING PROGRAMMABLE ANALOG FUNCTIONS AND COMPUTER AIDED TECHNIQUES FOR PROGRAMMING THE CIRCUIT	Nov. 30, 1995

OTHER DOCUMENTS

Goodenough, F. "Analog Counterparts of FPGAS Ease System Design" Electronic Design, Penton Publishing Cleveland, OH, US vol. 42, no. 21, 10/14/94, pages 63-64, 66,68,7 XP000477345 ISSN: 0013-4872 the whole document.

Goodenough, F. "Analog Counterparts of FPGAS Ease System Design" Electronic Design, Penton Publishing Cleveland, OH, US vol. 42, no. 21, 10/14/94, pages 63-64, 66,68,7 XP000477345 ISSN: 0013-4872 the whole document.

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Attorney Docket No.: CYPR-CD00232

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Snyder

Group Art Unit: 2183

Filed: October 22, 2001

Examiner: PAN, Daniel H.

Application No.: 10/033,027

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Title: PROGRAMMABLE SYSTEM ON A CHIP

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	5,399,922	3/21/95	Kiani et al.	326	40	7/2/93
	B	5,680,070	10/21/97	Anderson et al.	327	336	2/5/96
	C						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	L	0450863A2	10/9/91	EPO	G11C	27/02		
	M	0499383A2	8/19/92	EPO	H03K	19/177		
	N	0308583 A2	3/29/89	EPO	G06J	1/00		
	O	069816A2	2/22/95	EPO	G06J	1/00		
	P	1170671A1	1/8/02	EPO	G06F	17/13		
	Q	95/32478	11/30/95	PCT	G06F	17/50		

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	R	Goodenough, F. "Analog Counterparts of FPGAS Ease System Design" Electronic Design, Penton Publishing Cleveland, OH, US vol. 42, no. 21, 10/14/94, pages 63-64, 66,68,7 XP000477345 ISSN: 0013-4872 the whole document.
	S	Harbaum T. El. Al: "Design of a Flexible Coprocessor Unit" Proceedings of the Euromicro Conference, XX XX, Sept. 1999, pages 335-342, XP000879556, page 337, right-hand column, line 13-page 338, left hand column, line 4; figure 1.

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.